Abstract—In this paper a design and implementation of the digital phase-locked loop (DPLL) using 45nm sub-micron CMOS technology is presented. The circuit design of the DPLL, which consists of a Phase frequency detector, voltage controlled oscillator (VCO), Divider network and loop filter, is introduced and the simulation results are given. The details of design theory and calculation are also described. The presented design has frequency range of 15 MHz - 365MHz operation with center frequency of 200MHz, lock time of approximately 350ns. The lock time was reduced by adjusting the loop filter capacitor. Simulations using BSIM4 45nm CMOS technology shows that a wide capture (acquisition) range from 91.05 MHz to 358.04MHz is achieved. The power dissipation at the center frequency is 3.39752µW at supply voltage of 0.8V.

Index Terms—PLL, PFD, DPLL, CMOS.

I. INTRODUCTION

In high speed communication systems, to make sure clock recover and synchronization by PLL is a most important factor of the systems, while in digital signal processing circuit, frequency synthesizer consisting of digital phase-locked loop has become a key part which is used for system clock inside chips. Phase locked loops (PLLs) are widely used in microprocessors and digital systems for clock generation and as a frequency synthesizers in communication systems for clock extraction and generation of a low phase noise local oscillator. A phase-locked loop is a feedback control circuit. As the name suggests, the phase locked loop operates by trying to lock to the phase of an input signal through the use of a negative feedback path. A basic form of a PLL consists of three fundamental blocks, as shown in figure 1.

- Phase frequency detector (PFD).
- Loop filter.
- Voltage controlled oscillator (VCO)
- Divider network

The phase detector compares the phase of a periodic input signal against the phase of the VCO. Output of the PD is a measure of the phase difference between its two inputs. The difference voltage is then filtered by the loop filter and applied to the VCO. The control voltage on the VCO changes the frequency in a direction that reduces the phase difference between the input signal and the local oscillator.

When the loop is locked, the control voltage is such that the frequency of the VCO is exactly equal to the average frequency of the input signal. As long as the initial difference between the input signal and the VCO is not too big, the PLL eventually locks on to the input signal. This period of frequency acquisition, is referred as pull-in time, this can be very long or very short, depending on the bandwidth of the PLL. The bandwidth of a PLL depends on the characteristics of the phase detector, voltage controlled oscillator and on the loop filter.

![Block diagram of DPLL](image-url)

Fig: 1.Block diagram of DPLL.

II. PHASE FREQUENCY DETECTOR

The phase frequency detector, measures the difference in phase between the reference and feedback signals. If there is a phase difference between the two signals, it generates up or down synchronized signals to the charge pump/low pass filter. To take care of these disadvantages, we implemented the Phase Frequency Detector, which can detect a difference in phase and frequency between the reference and feedback signals. Also, unlike the XOR gate PD, it responds to only rising edges of the two inputs and it is free from false locking to harmonics. The PFD design uses two flip flops with reset features. The inputs to the two clocks are the reference and feedback signals. The D inputs are connected to VDD always remaining high. The outputs are either UP or DOWN pulses. These outputs are both connected to an AND gate to the reset of the D-FF’s. When both UP and DOWN are high, the output through the AND gate is high, which resets the flip flops. Thus both signals cannot be high at the same time. This means that the output of the PFD is either an up or down pulse but not both. The difference in phase is measured by whichever rising edge occurs first. As shown in figure 8 the implementation of
Phase Frequency Detector in 45nm CMOS technology which is used in PLL to lock the phase and frequency of the feedback signals with reference clock signal. The phase difference between the dclock and data is given by
\[
\Delta \phi = \phi_{data} - \phi_{dclock} = \frac{\Delta t}{T_{dclock}} \cdot 2\pi \text{ (radians)}
\]
...(1)

\[V_{p_{dtr}} = \frac{V_{DD} - 0}{4\pi} = K_{p_{dtr}} \Delta \phi \] ...(2)

\[K_{pd} = \frac{V_{DD}}{4\pi} \] ...(3)

As shown in figure 2 & 3 the implementation of Phase Frequency Detector in 45nm CMOS technology which is used in PLL to lock the phase of the feedback signals with reference clock signal. In figure 3 the simulation result of Phase Frequency Detector at \(\Delta \phi = \pi / 2\) is given.

Fig: 2. Implementation of Phase frequency Detector

III. LOOP FILTER

The function of the loop filter is to convert the output signal of phase frequency detector to control voltage and also to filter out any high frequency noise introduced by the PFD. The loop filter used with this type of PFD is a simple RC low-pass filter. Since the output of the PFD is oscillating, the output of the loop filter will show a ripple as well, even when the lock is locked. This modulates the clock frequency, an unwanted characteristic of a DPLL using PFD. A ripple on the output of the loop filter with a frequency equal to the clock frequency will modulate the control voltage of the VCO.

IV. CURRENT STARVED VCO

A voltage controlled oscillator (VCO), which is a nonlinear device, which produces an oscillation whose frequency is controlled by the voltage from the loop filter. In PLL system, the output of loop filter is connected to the input of the VCO. Voltage controlled oscillators are means of the generation of periodic signals in circuits. The VCO output frequency is approximately has a linear proportion with the input voltage from the loop filter. Therefore, changing the applied voltage to the VCO results the variable frequency output of a VCO. Consider the typical characteristics of VCO shown in figure 4. The frequency of the square wave output of the VCO is \(f_{center}\) when \(V_{in} = V_{center}\) is VDD/2 (typically). The other two frequencies of interest are the minimum and maximum oscillator frequencies, \(f_{min}\) and \(f_{max}\) possible, with input voltage \(V_{min}\) and \(V_{max}\), respectively.

It is important that the VCO continue to oscillate with no input data. Normally, the VCO is designed so that the nominal input data rate and the VCO center frequency are the same. This minimizes the time it takes the DPLL to lock. The gain of the VCO is simply the slope of the curve given in figure 4. This gain can be written as

\[K_{VCO} = 2\pi \cdot \frac{f_{max} - f_{min}}{V_{max} - V_{min}} \text{ (radians / s \cdot V)} \]
...(7)

VCO Specifications:

\[V_{DD}=1V,\]
\[l_n = l_p = 1\]
\[W_n = 10, \quad W_p = 20,\]
\[t_{ox} = 14A\circ, \quad \varepsilon_0 = 8.85 \text{ aF/\mu m, } \varepsilon_r = 3.97\]
\[I_D = 10 \mu A\]
\[f_{osc} = 200MHz.\]

We begin by calculating the total capacitance.

\[C_{tot} = \frac{5}{2} \cdot 25 \frac{R_{unim}}{um^2} \cdot (20.1 + 10.1) \cdot (0.045 \text{ um}^2) = 3.77 \text{ fF} \] ...(8)

Let's use a centre drain current of \(10 \mu A\) based on \(I_D = V_{ISO}\) characteristics of the MOSFETs. The selection of the current is important because when \(V_{iso}\) is VDD/2, the oscillation frequency to be 200MHz. The number of stages, is

\[N = \frac{I_D}{V_{DD} C_{tot} f_{osc}} = \frac{10 \mu A}{200 \text{ MHz} \cdot 3.77 \text{ fF} \cdot 0.8} \approx \ldots \] ...(9)
Total 17 stages are required to generate 200MHz oscillating frequency at the control voltage of approximately VDD/2. The gain of the VCO after liberalizing is calculated

\[ K_{\text{VCO}} = 4.641 \times 10^9 \text{ (radians / s \cdot V)} \]  

As shown in figure 5 the implementation of Current Starved VCO in 45nm CMOS technology which is used in PLL to oscillate at control voltage generated by loop filter. In figure 6 the simulation result of Current Starved VCO at 400mV control voltage is given.

![Fig: 5. Implementation of Current starved VCO](image)

V. DIVIDER NETWORK

The divider network is feedback given to the XOR phase detector. Here we used divide by 2 network, we can vary the divider network for synthesis of different frequencies. It divide the clock signal of VCO and generate dclock as shown in figure 7 & 8, than applied to XOR phase detector which compare it with input data.

![Fig: 6. Simulation result of VCO at 400mV V\text{inVMCO}](image)

VI. IMPLEMENTATION OF DPLL

The implementations of DPLL after the integration of all blocks of PLL are shown in figure 9. The transient analysis of DPLL is shown in figure 10, from this figure we have measured the settling time or lock time of the DPLL, and it is approximately 25 ns. Means that the phase of the output and input frequency is locked. The sky blue waveform in figure 10 shows the input control voltage of VCO or output of the loop filter. The DPLL specification shows in table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>45nm CMOS (BISIM4)</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>0.8v</td>
</tr>
<tr>
<td>Output frequency range</td>
<td>15MHz – 365MHz</td>
</tr>
<tr>
<td>Center frequency</td>
<td>200MHz</td>
</tr>
<tr>
<td>Capturing range</td>
<td>91.05MHz – 358.04MHz</td>
</tr>
<tr>
<td>Lock time</td>
<td>350Ns</td>
</tr>
<tr>
<td>Power consumption</td>
<td>3.39752\mu W</td>
</tr>
</tbody>
</table>
Based on this paper we can again improve the performance and parameters by using charge pump instead of tri-state device with PFD, my future work was to increase the operating frequency up to 1GHz with charge pump PFD.

REFERENCES


AUTHOR’S PROFILE