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Sub-degree phase-tuning capability using DDS in Digital Down Converter

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***Abstract*- This paper presents the digital architecture of DDS eliminates the need for the manual tuning and tweaking related to component aging and temperature drift in analog synthesizer solutions, The DDC (Digital Down converter) has become a cornerstone technology in communication systems. Digital down Converter (DDC) is key component of RF systems in communications, sensing, and imaging. To extract the band of interest at the high sample rate would require a prohibitively large filter. Xilinx provides a free DDC core. A DDC consists of cascaded integrated comb filter, a mixer and direct digital synthesizer (DDS).**

Index Terms- Theory of DDC, Direct Digital Synthesizer (DDS), Advantages of DDS, Results

I. INTRODUCTION

Digital down Converter (DDC) is key component of RF systems in communications, sensing, and imaging. Digital radio receivers often have fast ADC converters to digitize the band limited RF or IF signal generating high data rates; but in many cases, the signal of interest represents a small proportion of that bandwidth. To extract the band of interest at this high sample rate would require a prohibitively large filter. A DDC allows the frequency band of interest to be moved down the spectrum so the sample rate can be reduced, filter requirements and further processing on the signal of interest become more easily realizable. A fundamental part of many communications systems is Digital Down Conversion (DDC). A Digital down Converter is basically complex mixer, shifting the frequency band of interest to baseband. The DDC is typically used to convert an RF signal down to baseband. It does this by digitizing at a high sample rate, and then using purely digital techniques to perform the data reduction.

A. Overview of the DDC implementation

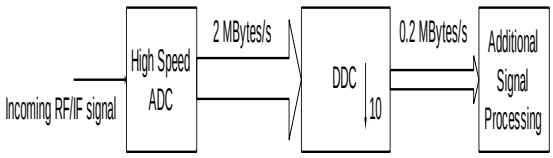

Figure 1 Overview of the DDC Function

Consider a signal lying in the range 10-20 KHz. The signal bandwidth is 10 KHz. However, it is often digitized with a sampling rate over 1 M samples per Second, representing in the region of 2Mbyte/second. The DDC allows us to select the 10-20 KHz band, and to shift its frequency down to base-band and in doing so reduce the sample rate, with a 10 KHz bandwidth, a sample rate of 100 KHz would be fine - giving a data rate of only 0.2Mbyte/second. This is shown in Figure 1.

II. DDS (DIRECT DIGITAL FREQUENCY SYNTHESIZER)

The DDS (DDS synthesizer) is an implementation of a direct digital frequency synthesizer (DDS) (also called Number Controlled Oscillator, NCO) which produces a sine wave at the output with a specified frequency and phase (adjustable at run time). The resolution of the Frequency Tuning Word (FTW), the phase and the amplitude are defined separately. While the FTW resolution can be set by the generic ftw_width, phase and amplitude resolution are defined as constants phase_width and ampl_width in the separate package sine_lut_pkg. This is generated by a Matlab script (sine_lut_gen.m), the m-files are described in their headers. The nomenclature of the files is sine_<phase_width>_x_<amplitude_width>_pkg. hd. By adding one of these files to the project, the resolution of phase and amplitude is automatically defined. The function of the DDS is to generate the frequency equal to the sampling frequency of the first stage. The figure 2 shows the implementation of the DDS. A direct digital synthesizer operates by storing the points of a waveform in digital format, and then recalling them to generate the waveform. The rate at which the synthesizer completes one waveform then determines the frequency [1], [2].

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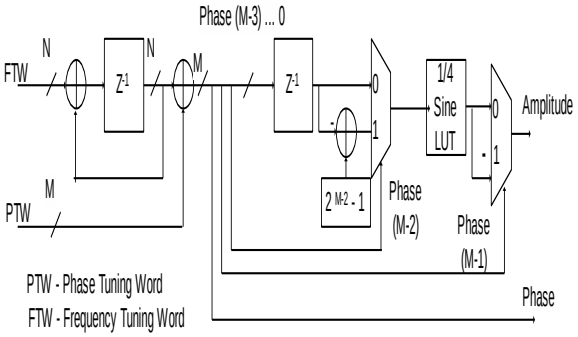

Figure 2 Direct Digital Frequency Synthesizer

A. Performance Details of DDS

The frequency and phase of the DDS can be controlled using the FTW (Frequency Tuning Word) and PTW (Phase Tuning Word).
The output frequency will be determined by the FTW.
$\mathbf{F_{dds}} = (FTW/2^{(N-M)})*(F_{clk} / (2^{M}))$ or
$\mathbf{F_{dds}} = FTW*F_{clk}/2^{N}$
Where F_{clk} = Clock Frequency
The initial phase can be controlled by PTW.
$\mathbf{\Phi_{dds}} = (PTW/2^{M})*2*pi$
Match the DDS frequency to the sampling frequency so that the spectrum gets shifted towards DC (0 Hz).

B. Advantages of DDS

Today's cost-competitive, high-performance, functionally integrated DDS ICs are becoming common in both communication systems and sensor applications. The advantages that make them attractive to design engineers include [7]:
1) Extremely fast hopping speed in tuning output frequency (or phase); phase-continuous
frequency hops with no overshoot/undershoot or analog-related loop settling-time anomalies,
2)The digital control interface of the DDS architecture facilitates an environment where systems can be remotely controlled and optimized with high resolution under processor control. Design and FPGA Implementation of High Speed, Low Power Digital up Converter for Power Line Communication Systems.

III. RESULTS

A. Simulation results for DDS

Sampling Frequency : 60 MHz

Table 1: Parameters used for DDS module:

Parameter	Parameter Name	Data Types	Value	Units
Frequency Tuning Word	FTW_WIDTH	Integer	11	Bits
Phase Tuning	PHASE_WIDTH	Integer	9	Bits
Word				
Output Amplitude Word	AMPL_WIDTH	Integer	16	Bits

Table 2: VHDL simulation results are shown below.

Frequency Required	FTW	FTW actual	Frequency Generated	Actual Frequency from Simulation	Results
10MHz	341.3333	341	9.99MHz	9.978MHz	Figure 3
15MHz	512	512	15MHz	15.000MHz	Figure 5

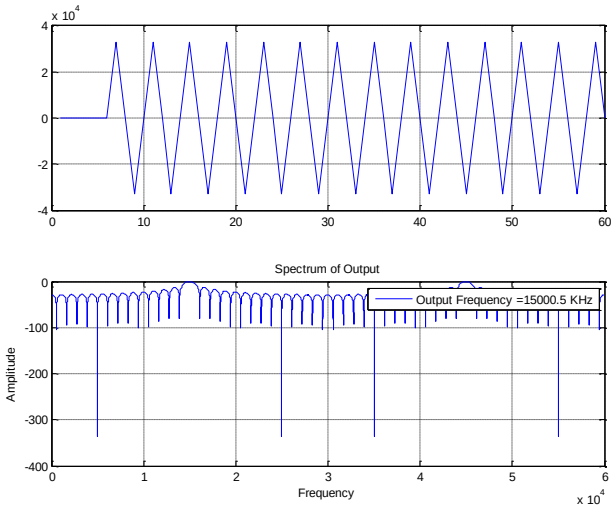

Figure 3

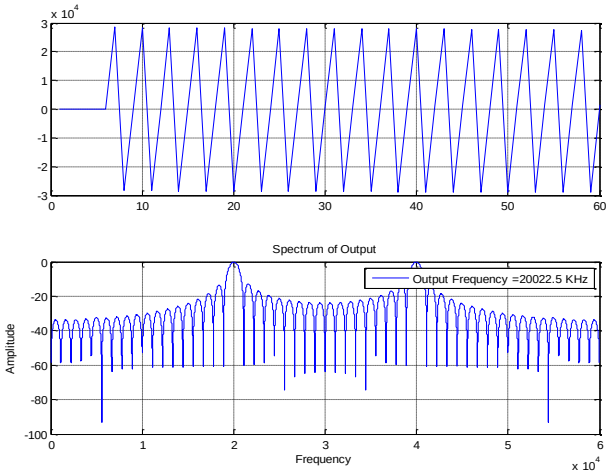

Figure 4

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IV. CONCLUSION

This paper deals with the development of a Digital down Converter for Communication system equipment. DDC performs mixing to shift the signal spectrum from the selected carrier frequencies to base-band, decimation to reduce the sample rate, and filtering to remove adjacent channels and minimize aliasing. Here DDS has digitally controlled micro-hertz frequency-tuning and sub-degree phase-tuning capability.

In the course of doing the project, insight knowledge has been gained into various fields like

- The Virtex II Pro FPGA architecture.
- Coding using Verilog.
- Digital signal processing concepts.
- Network and communication concepts.
- Tools such as Xilinx ISE, ModelSim, and Matlab and Xilinx system generator.

V. FUTURE WORK

With a DDC, if the system operates at all, it works perfectly – there's never any tuning or component tolerance to worry about. As rate is programmable, then amplitude modulation can achieve with DDC in communication system. The design of code requires hardware with more resources as it exceeds the capacity of lower FPGA devices.

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