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TESTING OF ADCs WITH DIGITAL ERROR CORRECTION BASED ON LINEARITY TEST METHOD

V.POONGUZHALI, *PG Scholar*, **P.MEENAKSHI VIDYA,** *M.E, Asst.Prof (SL.GR)*

***Abstract*— Analog to digital conversion is an important way of interpreting the real time signals into digitally understandable form, Operation of various digital media devices depends on the accurate information provided by its ADC unit like GPS operated devices, smart phones, Accelerometer etc. In existing Histogram based ADC error detection, the concept of code density is rather cost consuming which increase the linearity testing time. This work proposes an transition code error detection in a multi stages pipelined ADC circuit which greatly reduces the linearity testing time. Instead of measuring every digital code generated, the integral and differential errors can be detected by converting the digital code into linear varying transition codes using a DFT analyzing circuit. The number of pipelined stages increases the circuit complexity but greatly reduces the testing time. A transition-code based method is used to reduce the linearity testing time of pipelined analog-to-digital converters (ADCs).In addition, a simple digital Design-for-Test (DFT) circuit is proposed to help correctly detect transition codes corresponding to each pipelined stage. A novel design of Hybrid pipelining method with both coarse and fine grain architectures will be design and compared for performance excellence.**

***Index Terms*— Histogram based ADC, transition code, DFT (Design-for-Test) circuit.**

I. INTRODUCTION

Analog to Digital Converters (ADCs) are widely used electronic components which often limit the performance of modern signal processing systems. Analog signals have an infinite number of output states, whereas digital outputs have a finite number of states[1]. There has been a significant effort to improve device performance, particularly for components used in wireless applications. Performance gains can be realized by at least three different methods[2].Large gains are possible by improving device characteristics. This can be realized by using advanced processes that define today's evolving electronics manufacturing technology[3]. A second method is by improving circuit design technologies or ADC architectures. Advances and changes in circuit design may be able to provide the lacking dynamic range of current ADCs. A final method is by calibrating and compensating existing devices. Using current devices with compensation provides additional gains for existing technology.

Analog signals are directly measurable quantities. Digital signals only have two states. For digital computer, we refer to binary states, 0and 1.ADC compensation is especially beneficial for wide-bandwidth receivers that require a large dynamic range of operation. This chapter presents a contextual description of the problems dealt within the work: analog-digital converters (ADC)s error characterization and modeling, pipeline ADC calibration, and wireless channel estimation and modeling[4]. The problem statements and formulations are presented as follows.

A calibration and compensation scheme is known as dynamic compensation if the dynamic nature of the input signal is accounted for in the compensation procedure. These types of compensation schemes have been successful in providing increased spurious free dynamic range (SFDR) in current ADCs. Dynamic compensation requires the ADC to be calibrated in order to obtain representations of the errors involved. Information about the error functions is then used to compensate the ADC by removing the error from the ADC output samples. A variety of calibration methods have been investigated. Some examples of ADC usage are digital volt meters, cell phone, thermocouples, and digital oscilloscope.

This work will concentrate on pipeline architecture ADCs, which have become the architecture of choice for high speed and moderate to high resolution devices. These devices are particularly important in wireless receiver applications because pipeline ADCs have moderate resolution, high speed and consume low power[5]. However the dynamic range of operation is often limited in current pipeline designs. The proposal of this work is to use the intermediate stage output bits in the compensation scheme. This work focuses on defining these errors and demonstrate, that these errors can be compensated using intermediate stage outputs. This work also defines a calibration scheme unique to pipeline ADCs.

The rest of the paper is organized as follows. Section II introduces error contribution in pipelined ADCs. Section III describes the pipeline ADC architecture. Section IV shows the comparison between histogram and transition code method. Section V is based on digital error correction method with the complete test procedure in detail. Section VI explains the simulation result of phase 1. Finally, the conclusions are given in section VII.

II. ERROR CONTRIBUTIONS IN PIPELINE ADCS

This section addresses possible error mechanisms that can be present in a pipeline converter. Extensive work has been done on characterizing error mechanisms and an overview can be found. Pipeline Analog-to-Digital data converters have many potential error sources.Many of them are the same error source found in other ADCs.

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There is, however fundamental difference in how the error sources appear in the final converted signal for pipelined ADCs. The segmented nature of the Pipeline ADC is very helpful in addressing power and speed concerns, but complicates understanding and reduction of error propagation from stage to stage. Simple errors in Pipeline ADCs produce non-linearities that are difficult to correct.The following paragraphs discuss error in the offset error,gain error,non-linear error,S/H and sub-ADC.

A. *Offset Errors:*

Offset errors are simple additive errors that can be modeled as an error constant summed with the signal. Offset errors in analog-to-digital converters are generally not difficult to compensate for especially when the offset propagates directly to the output. In such a case, a simple system-level calibration can correct this error. Common offset sources in Pipeline ADCs are charge injection, opamp offset and finite gain, comparator offset, and DAC offset.

B. *Gain Error:*

Gain error is a multiplicative error that acts on the input signal. It can be modelled as a gain stage where a gain of one is the optimal gain value. Like offset error, gain error on the system level is a fairly simple error to correct. Also, just like offset error within pipelined stages, gain errors can create difficult-to-remove non-linear errors. The most common gain error sources are feedback capacitor to DAC capacitor mismatch and under-settled discrete-time signals.

C. *Non-Linear Error:*

Linearity is simply defined as a property of a system whereby the input-to-output characteristic is wholly linear and can be described in the form $y = mx + b$. There are also some error sources in Pipeline ADCs that are inherently non-linear. These are opamp output non-linearity, signal-dependant switch resistance, and non-linear capacitance.

D. *Sample and Hold Error:*

The S/H is the first block in each stage, and determines the actual input signal bandwidth for the converter. S/H error can be modeled as a small change in the ideal input sample X. Let the held sample be represented as X+_X. The M and N-bit ADC can be used to show the effects of the sample error component _X at various points in the pipeline architecture. Refer to figure1 .

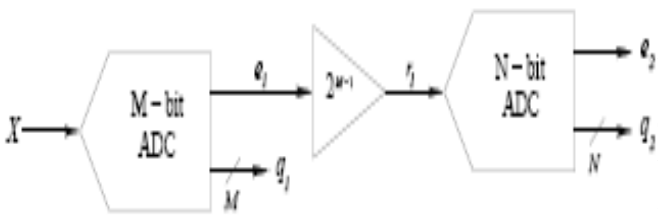

Figure 1 : An N-bit ADC connected to an M-bit ADC.

III. PIPELINE ADC

A pipeline ADC (also called subranging quantizer) uses two or more steps of subranging. First, a coarse conversion is done. In a second step, the difference to the input signal is determined with a digital to analog converter (DAC). This difference is then converted finer, and the results are combined in a last step. This can be considered a refinement of the successive-approximation ADC wherein the feedback reference signal consists of the interim conversion of a whole range of bits (for example, four bits) rather than just the next-most-significant bit. By combining the merits of the successive approximation and flash ADCs this type is fast, has a high resolution, and only requires a small die size.

The pipelined is a popular architecture for modern applications of analog-to-digital converters due to its high sustained sampling rate, low power consumption, and linear scaling of complexity. Figure 2 shows a block diagram of a pipelined ADC. The term “pipelined” refers to the stage-by-stage processing of an input sample VIN.

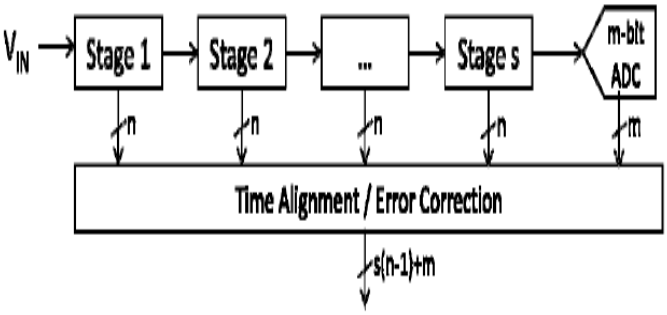

Figure 2: Pipelined ADC Block Diagram

In the above diagram, the analog input voltage VIN enters the ADC. Each subsequent pipeline stage of ADC resolves a certain n number of bits to be contributed to the final conversion output. The number of bits that each stage is responsible for quantizing is usually on the order of 1 – 5 bits. Simultaneously, after each stage has finished quantizing its input sample to n bits, it outputs an analog residue voltage that serves as the input to the next stage.

After s stages of conversion, an m-bit ADC resolves the lower bits of the overall ADC digital output. Each stage’s digital decision is then passed to a digital block that properly time-aligns the output bits and corrects for any errors in each stage. The final digital decision is then produced.

The successive approximation ADC method is stated into transfer model and the transfer function are splitted into n pipelined stages.Each computations are performed as (coarse) large computation.Execution in pipelined stages and the individual pipeline stage output are grouped into digital output.

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A. *COARSE GRAIN:*

System will do large amount of computation before reporting is called as coarse grain. Major instruction sets are splitted into parallel operating instruction steps (s1,s2,s3….etc). Each steps contains sub operation like loops , dependent instruction etc.

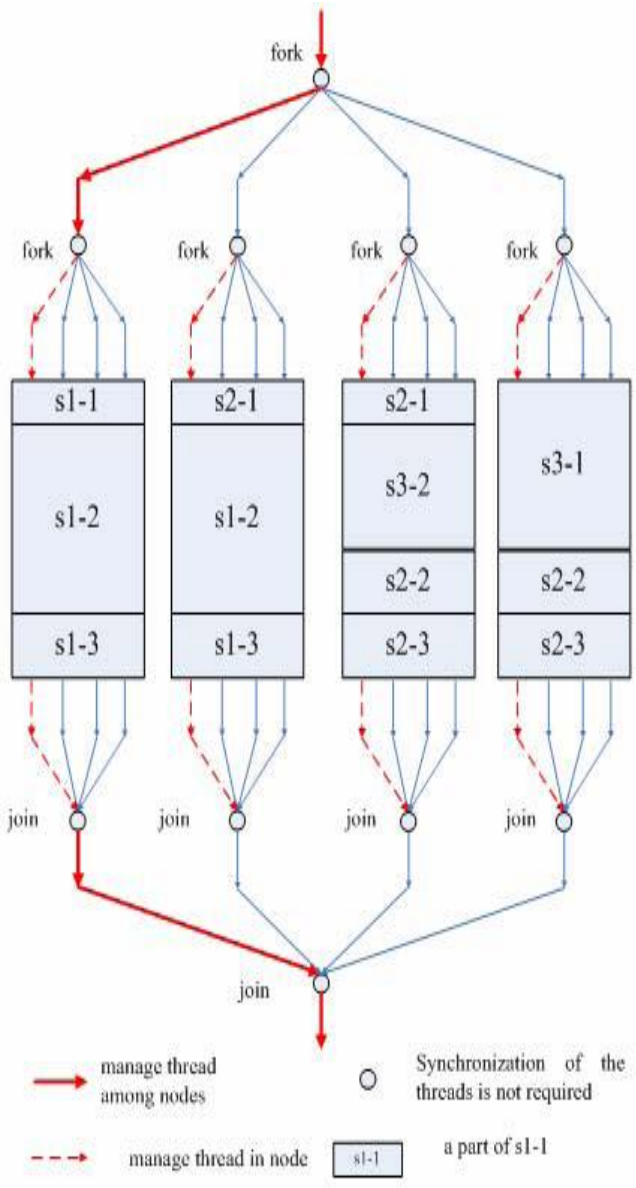

Figure 3:Coarse Grain Execution Model

B. *FINE GRAIN:*

System will do small amount of computation before transferring. The already coarse grain splitted steps are further categorized into sub steps and executed with inner fine grain architecture.

The dependent instruction cycles are adjusted to wait for the running instruction to complete.

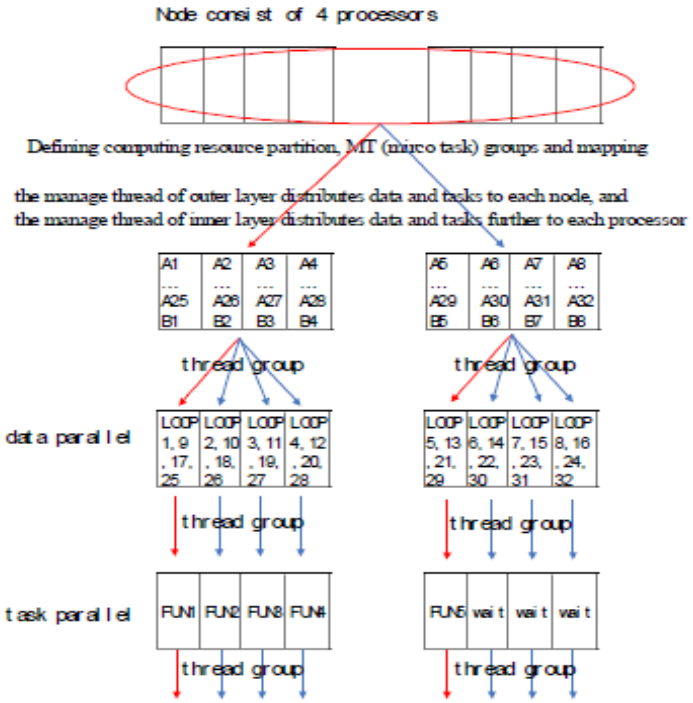

Figure 4: Fine Grain Execution Model

Calculation involving analog to digital conversion will be stated and categorized.The categorized mathematical operation will be scheduled.The mathematical expression are sub scheduled as fine grain instruction.For example a multiplication can be converted into repeated additions.Based on the coarse grain and fine grain prediction a VLSI architecture will be developed by hybriding both pipelined architecture.

C. *12 Stage Pipelined ADC:*

To select proper transition codes of each stage significantly determines the testing accuracy of the proposed method. In the overlapped region of Fig. 5,transition codes of the target pipelined stage are possible to be the same with those of previous stages. Under this situation, the overlapped transition codes contain nonlinearities of previous stages, and the nonlinear error effect of target stage cannot thus be correctly identified. When the overlapped transition codes are selected and their measured results are duplicated for other transition codes of the target stage, the nonlinear effects of previous stages are also duplicated. As a result, the test accuracy of the proposed method is seriously degraded.To avoid this condition, the first and the last sets of transition codes of each stage, out of the overlapped region, are selected.These transition codes are impossible to be the same with those of previous stage when comparator offset does not exceed the tolerable value of DEC. The selected transition codes of the first three stages are marked with “ ” symbol in Fig. 5.

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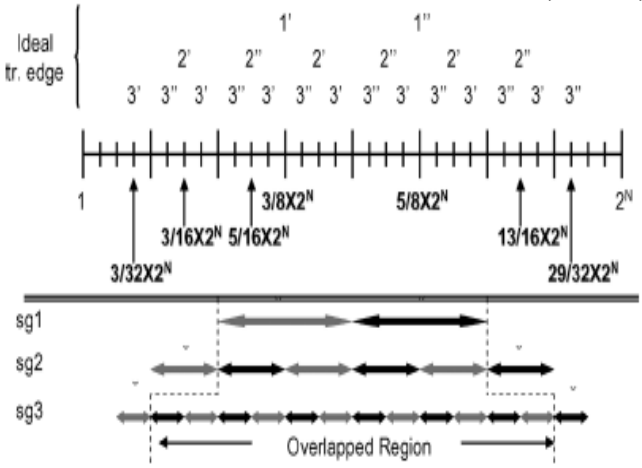

Fig. 5. Concept diagram for the distributions of transition codes corresponding to the first three 1.5-bit stages.

IV. HISTOGRAM VS TRANSITION CODES

A. *Histogram Method:*

In , a histogram is a graphical representation of the distribution of data. It is an estimate of the probability distribution of a continuous variable and was first introduced by Karl Pearson. A histogram is a representation of tabulated frequencies, shown as adjacent rectangles, erected over discrete intervals (bins), with an area equal to the frequency of the observations in the interval[7]. The height of a rectangle is also equal to the frequency density of the interval, i.e., the frequency divided by the width of the interval. A histogram may also be normalized displaying relative frequencies. It then shows the proportion of cases that fall into each of several categories, with the total area equaling 1.The categories are usually specified as consecutive, non-overlapping intervals of a variable. The categories (intervals) must be adjacent, and often are chosen to be of the same size. The rectangles of a histogram are drawn so that they touch each other to indicate that the original variable is continuous. Histograms are used to plot the density of data, and often for density estimation: estimating the probability density function of the underlying variable. The total area of a histogram used for probability density is always normalized to 1. If the lengths of the intervals on the x-axis are all 1, then a histogram is identical to a relative frequency plot.

B. *Transition code method:*

Transition coding is a upcoming method used to reduce the possible error occurrence in a ADC.A transition code based

method is proposed to reduce the linearity testing time of pipelined ADC[8].A transition codes corresponding to each pipelined stage are shifted by comparator offsets and also at each stage are difficult to estimate.

C. *Flow of Work:*

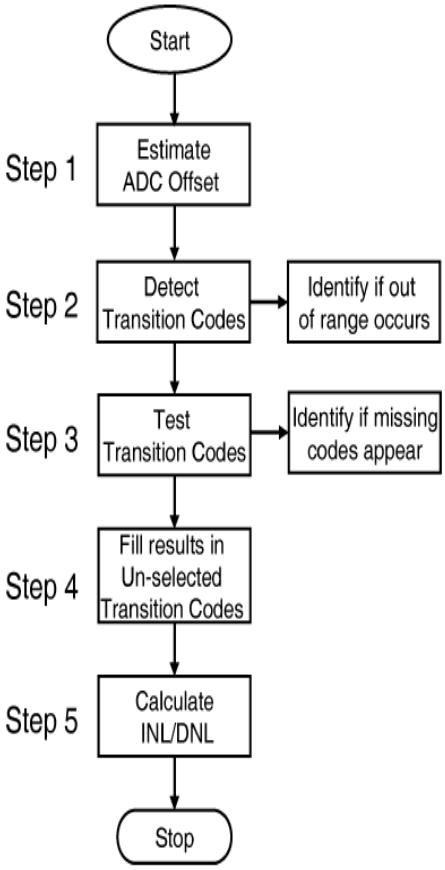

Figure 6: Test procedure of proposed transition code based method

Step 1*:* ADC input affects the range of input stimulus for testing transition codes of each pipelined stage. Now the ADC offset is estimated. Step 2*:* The immediate range exceeding digital values are detected along with the conversion of transition codes. Step 3: The detected transition codes are grouped to find the missing code occurrence of each stage.Step 4: The test result of the un-selected codes are filled with those of selected test codes. Step 5: When CBWs (code bin width) of all ADC codes are determined, the corresponding DNL and INL calculations are performed[9].

V. DEC TECHNIQUE

The DEC technique has been applied to relax the comparator offset requirement in pipelined ADC. In this paper, DFT circuit is introduced to assist in detecting transition codes of pipelined stages in ADC with DEC technique. DEC is an adjustment circuit which is capable of detecting single bit errors present during analog to digital conversion.

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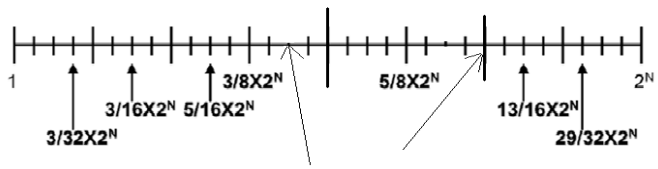

Figure 7: Ideal Case Of Transition Edge

In this paper various pipeline stages are used for analog to digital conversion and simple paring based DEC will take place on each pipelined stage.

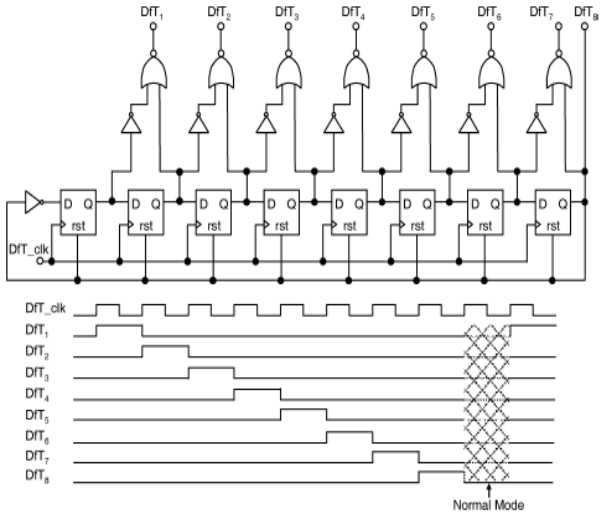

Figure 8: DEC Logic Diagram

VI. A SIMULATION RESULT

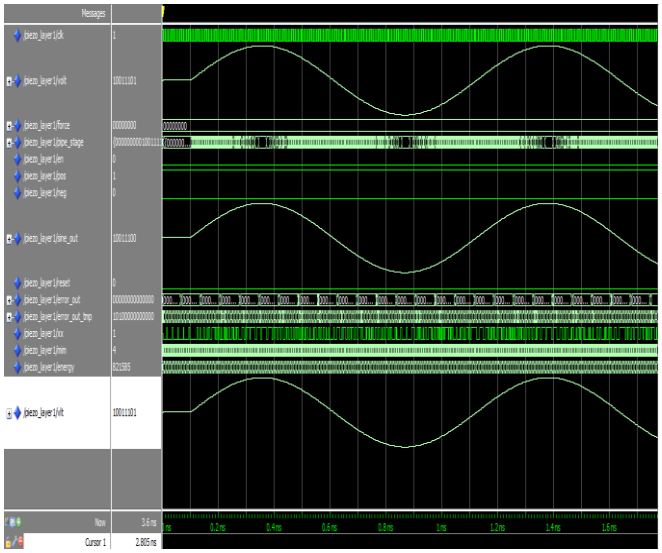

Figure 9: ADC digital error correction graph

A 32-bit pipeline stages for ADC conversion is designed and each pipeline stages output is converted into equivalent transition codes. The design of transition code based ADCdigital error correction is successfully designed by using modelsim simulation tool and the result graph is shown above.The initial analog input of volt is generated as input, the 32 level 16 bit Pipeline stages are employed for parallel analog to digital conversion. The calculated digital ADC offsets are converted into equivalent transition codes which shown in the variable xx from the above graph. The transition codes are further tested for missing and out of range codes. The sine out variable holds the differential Non linearity corrected output and the variable 'vlt' holds the integral corrected output.

VII. CONCLUSION AND FUTURE WORK

Thus a successful recovery of the original analog signal is acquired using DFT digital error detection and correction circuitry. Coarse grain pipeline stages has the capability to convert and correct coarse analog values whereas it can't produce accurate result for fine analog values. Here fine grain pipeline stages will be combined with coarse grain pipeline stages to tune either coarse grain or fine grain analog values. The coarse grained multi pipelined staged ADC can be scheduled into fine grain pipelined tuning which will further increase the accuracy and reduces the delay time with a trade of area coverage.

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Authours Biblography

V.Poonguzhali received bachelor of Engineering degree in Electronics and Communication from Anna University, India. She is pursuing her master of Engineering in VLSI Design in Easwari Engineering College . Her research interest includes Testing of VLSI circuits and Signal processing.

Meenakshi vidya. P pursued her B.E. Degree in Electronics and Communication Engineering at University of Madras, Chennai, and received her M.E Degree in VLSI Design from Anna University, Chennai, India. She is currently working as Assistant Professor at Easwari Engineering College, Chennai, India. She has published more than 25 papers in National and International Conferences. She is a member of IEEE & ISTE professional chapters.