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Multiple Scan Methodology for Detection and Tuning Small Delay paths

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***Abstract*—Digital life standard demands accuracy which requires Enhanced VLSI architecture in every aspect. Various chip defect identification methods focuses on stuck and sequential faults, this work focuses on categorizing the chip by testing with three different testing scenarios. Detecting and categorizing Small delay defects often requires sophisticated experimental setup which involves complex test procedures. Detecting a small delay defect and categorizing it on a run time chip is time and cost consuming. This work proposes an AC scan delay testing methodology to assure three stages of test coverage verification with reduced hardware requirements, (i) Finding the longest critical path in a chip (ii) Categorization of defective chips which overlaps the longest time bound predicted, based on its probability of failure attempts (iii) Extracting the waveform of each flip flop stages for post fabrication steps. A VHDL modelling of test bench generation will be designed using Modelsim simulation tool, the percentage of fault coverage achieved by our proposed AC plus scan method will be tested in s298 benchmark circuit under three frequency ranges (target, middle and contour). This chip defect identification methodology can be further extended to fault tolerant methodology.**

***Index terms*—AC Scan, benchmark circuits, clustering, delay testing, small delay defects.**

I. INTRODUCTION

AS PROCESS dimension continues to shrink, delay testing becomes an important factor for achieving satisfactory product quality. There are many factors that could cause delay variation in a chip. For instance, random dopant fluctuation could cause threshold voltage mismatch between transistors and results in significant delay variation. Understanding the effectiveness of their production tests is a critical task for IC suppliers. Numerous trends have been introduced that conventionally applied test methods must change to meet future needs will make the task even more critical-and difficult-in the future. The characterization and diagnostic data and ideas aimed at helping IC suppliers understand test effectiveness [1]. There are two major strategies for delay testing. One is the *at-speed functional test*, by using functional patterns to test the chips at the target operating frequency. The at-speed testing maintains the test quality for larger, more complex chips and new fabrication processes. The Scan-based ATPG testing process for at-speed testing ensures high test coverage by optimizing it across multiple clock domains [2]. The other delay testing method is the *at-speed scan test*, also known as AC scan test. There are two fault models for generating AC scan test patterns. One is *path delay fault model* [3]. Path model considers the delay along the structural paths. High coverage of path delay faults can effectively detect small delay defects. Another fault model is the *transition fault model*. The feasible method of delay testing is the generation of test patterns and simulating the fault, which when used with parallel-pattern, single-fault propagation is an efficient way to simulate the delay faults [4]. By incorporating Standard Delay Format (SDF) files, into the ATPG tool improve the quality of test sets generated for detecting delay defects. The timing information is used to guide the test generator to detect faults through the longest paths in order to improve the ability to detect small delay detects [5]. Very deep sub-micron (VDSM) technologies are especially susceptible to process variations, crosstalk noise, power-supply noise, and defects such as resistive shorts and opens, which induce small delay variations in the circuit components. Such delay variations are referred as *Small-delay defects* (SDDs). By selecting the best set of test patterns for SDD detection from an n-detect pattern set generated using timing-unaware automatic test pattern generation (ATPG) [6]. The AC delay patterns, a carefully-selected, tighter clock would result in higher effectiveness to screen out the potential defective chips. Then, by using a smarter test clock scheme and combining with a second set of AC delay patterns, the overall quality of AC delay test can be enhanced while the cost of including the second pattern set can be minimized [7]. The testing of small delay defects incorporates the use of standard transition delay ATPG along with timing information gathered from standard static timing analysis (STA), in order to obtain high defect coverage of the small delay defects that lie along the critical paths [8]. The delay test for system on chip (SOC) devices with high frequency clock domains is used to reduce test vector count and to increase test quality [9]. To test timing related faults between synchronous clocks, an at-speed test clock and an automatic test pattern generation scheme are used in which the internal *phase-locked-loop* (PLL) as the at-speed test clock generator, which supports at-speed testing for inter-clock domain and intra-clock domain logic [10]. The delay testing method using one-class Support Vector Machine (SVM) that gathers all the information it needs is in the similarity matrix that records the similarity measure between every pair of samples using a polynomial kernel is most effective for detecting delay defects [11]. Each test pattern is characterized by the frequency that it will fail, called *failing frequency*. A *Failing Frequency Signature* (FFS) is a collection of maximum operating freq.of each pattern in pattern set.

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Analyzing the failing frequency signature can successfully detect small-delay defects [12]. In the output hazard free Transition Delay Fault (TDF) generation strategy relies heavily on the ability of generating multiple diverse TDF vectors for the same targeted TDF fault so as to maximize the probability of detecting the fault even if many of the tests are invalidated because of output hazards [13]. In our Ac-plus scan methodology, we can perform three test modes, namely: 1) delay measurement; 2) adaptive-frequency test; and 3) waveform extraction. Since each test pattern may have a distinct delay, we adapt the test frequency from one test pattern to another as well. This test mode introduces only a very modest test time overhead than the traditional AC-scan and thus it is efficient enough to be used for volume production test. Thirdly, we can extract the waveform of any selective flip-flop under any give test pattern, for the silicon debugging purpose.

II. Per-Pattern Delay Measurement

For measuring the delay of a test pattern, proposed a sweeping frequency method. For each pattern, the test frequency starts from a low value and incrementally increases until the test pattern fails. By that, one can record the failing frequency of each pattern, which also indirectly implies the longest path delay of the respective pattern. In this paper, we call this as delay measurement rather than collecting the failing frequency. The chip with its signature deviating from the normal region is considered as failing. AC-plus scan methodology in that we can adapt the test frequency conditionally at any moment based on the previous test responses of the CUT. There is time overhead in configuring but it is modest.

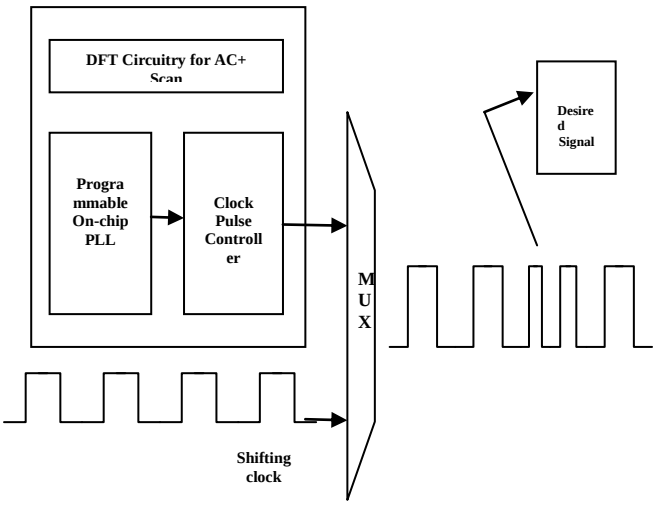

Fig. 1. Architecture of AC-plus scan.

First of all, we use the nominal delay plus 3 to 6 standard deviations as the starting test clock period for delay measurement. We refer to the added number of standard deviations as *measurement confidence*.

We employ an on-chip ALPLL to generate a wide range of test frequencies for delay testing in our AC-plus scan architecture as shown in Fig. 1. First the nominal delay for each pattern is calculated. This is done by computer simulation and it is termed as temporary nominal delay. The characteristic results found from the first passing chip can be used as temporary references for the next chip. This step continues until it covers the statistical nominal delay. The hazard-free patterns which are generated by aforementioned methods may not have adequate fault coverage; it is common that certain amount of non-hazard-free patterns is needed to further boost up the fault coverage. For non-hazard-free patterns, we could perform delay measurement by using binary search with a small possible range of each pattern. This smaller range of binary search is described in (1), where D_i is the nominal delay of pattern i, R is the measurement confidence and σ is the standard deviation.

$$\begin{aligned} Upper\ Bound: D_i * (1 + R\sigma) \\ Lower\ Bound: D_i * (1 - R\sigma). \end{aligned} \quad (1)$$

A. Delay Score

Delay Score is defined as the *total measured extra abnormal delay* for all patterns. Once the delay of a pattern exceed the contour test clock period, that pattern would be assigned a delay score corresponding to its abnormal delay. After we test all patterns, we add up all the delay scores of all patterns as shown in (2), the delay score for the chip. High delay score means there are plenty of abnormal delay in that chip. Where $Delay\ Score_i$ is delay score of pattern i, $D^i_{pattern}$ is the longest path delay of pattern i, $D^i_{threshold}$ is the threshold for normal process variation for pattern, and D_{unit} is the delay unit.

$$Delay\ Score_i = \frac{D^i_{pattern} - D^i_{threshold}}{D_{unit}}. \quad (2)$$

B. Delay Unit

Delay unit is the unit for the calculation of the delay score. We tend to use a delay unit that scales with designs. Hence, we define it as the *average of the standard deviations of all patterns*, as shown in (3), where D_{unit} stands for the delay unit, N stands for the total number of test patterns, and σ_i stands for the standard deviation of pattern.

$$D_{unit} = \frac{\sum_1^N \sigma_i}{N}. \quad (3)$$

III. Adaptive-Frequency Test

In our adaptive-frequency test, every pattern could at most tested by three test signals, including target test clock, middle test clock, and contour test clock. It is notable that

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the horizontal axis of this figure as shown in Fig. 2 is the index of the test patterns sorted by the longest path delay.

1) **Target Test Clock Period:** This is the inverse of the target operating frequency of the circuit under test.

2) **Contour Test Clock Period:** A contour test clock period for one pattern is simply its longest path delay plus some margin. *Testing a pattern with the contour test clock can be viewed as a special form of stress test, aimed at exposing any delay larger than the normal delay*.

3) **Middle Test Clock Period:** The middle test clock period of a pattern is simply the middle value of the target test clock period and its contour test clock period. This period also varies with the pattern like the contour test clock period.

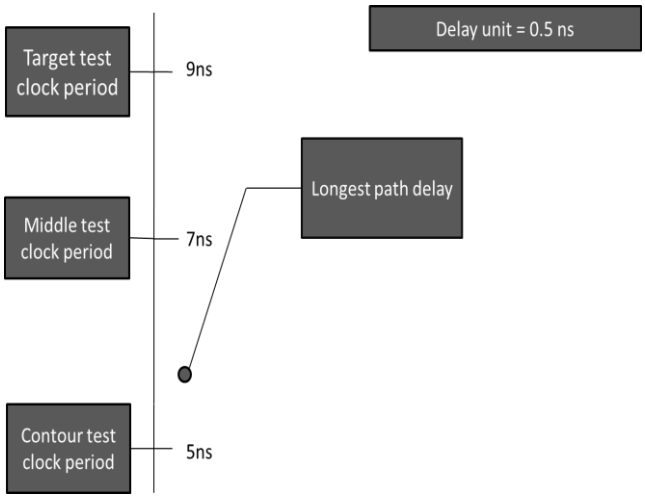

Fig. 2. Three types of test clock periods.

A. *Three Catagories Of Chips*

After performing the adaptive-frequency test, we will classify a chip into one of three categories as described in Fig. 3.

1) **Passing chips:** These chips pass for all patterns under the contour test clock period and the target test clock period. They can be viewed as robustly working devices.

2) **Failing chips:** These chips fail for at least one pattern under the target test clock period, which means that they could not meet the target timing requirement, and thus they should be treated as malfunctioning chips and discarded. Normally, these chips also fail the traditional at-speed scan test.

3) **Marginal chips:** These chips fail for at least one pattern at contour test clock period, but pass for all the other patterns at target test clock period. In some sense, their test results are in the ambiguous region between good and total failure. We refer to them as marginal chips. In this paper, we propose to grade these chips with a *delay score* and *unreliability score* to represent the levels of their marginalities.

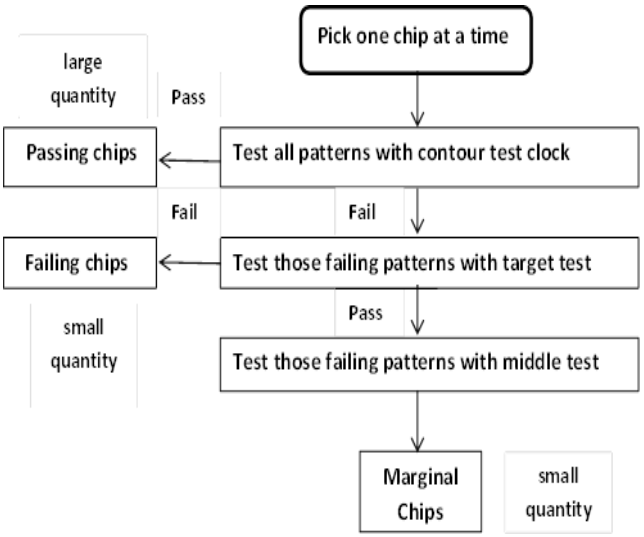

Fig. 3. Flow of adaptive-frequency test.

B. *Unreliability Score*

A marginal chip could be caused by spot defects in addition to extreme process variation. Studies have revealed that a spot defect may deteriorate and cause larger delay over the time during its usage in the field. That implies that an originally harmless small delay could become malicious or even catastrophic. In light of this, we define a term called unreliability score to measure the possibility of such reliability failure. It is shown in (4), where D_{target} is the target test clock period, $D^i_{pattern}$ is the longest path delay of pattern i. *It basically reflects the distance between the longest path delay of a pattern and the target clock period. The shorter this distance, the higher the unreliability score.*

$$\frac{D_{target}}{D_{target} - D^i_{pattern}}. \quad (4)$$

IV. WAVEFROM EXTRACTION

Silicon debug is an important phase in IC product development. It has been reported that this phase could take over 50% of the overall product development time. In the step of finding the "root cause of the failure," one usually uses special probing tools such as laser voltage probe (LVP) and laser assisted device alteration (LADA) to take waveforms from the circuit. When we apply those laser-based probing tools which would add extra heat to the chip. With AC-plus scan architecture, extract the waveform from each flip flop in real time those pins are the testing output pins then post silicon debugging and fabrication is done so that time period gets reduced and then area will be reduced.

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AC - plus scan test for chosen pattern with test frequency sweeping from 400 MHz down to100MHz.

V. Benchmark Circuit

The *s298 benchmark circuit* has the advantage of testing both parallel and sequential circuit errors, since it contain scan chain flip flops and feedback combinational circuits. The high-level *ISCAS-85* benchmarks discussed in this paper are used for finding the path delay errors and transition errors. The models, of which we have constructed both structural and behavioral versions, partition the original gate-level netlists into standard RTL blocks and identify the functions of these blocks. Together, the gate-level and high level models form a set of hierarchical benchmark circuits that have proven to be useful research tools in several areas of digital design, including test generation, timing analysis, and technology mapping. The s298 circuit consists of 3 inputs, 6 outputs, 14 D-type flip-flops, 44 inverters, 75 gates (31 ANDs + 9 NANDs + 16 ORs + 19 NORs). The ISCAS-85 benchmak circuits include s27, s208, s298, s347, s386, s510, s9234.

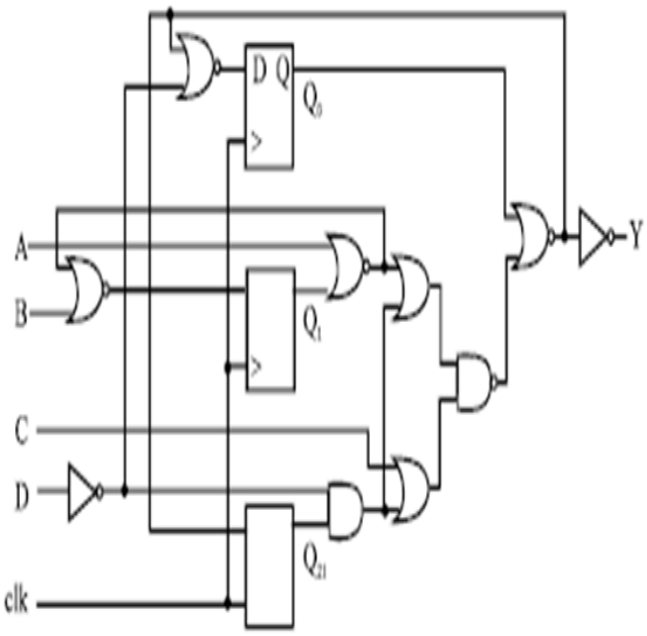

Fig. 4. An s27 Benchmark circuit

The s27 circuit consists of 4 inputs, 1 output, 3 D-type flip flops, 2 inverters, 8 gates (1 ANDs + 1 NANDs + 2 ORs + 4 NORs) as shown in Fig. 4.

The letter s signifies that the circuit is synchronous sequential; the number that follows represents the number of interconnect lines among the circuit primitives. Note that the double of this number also represents the upper bound on the size of the single stuck-at fault list. Experiments performed on the ISCAS-85 benchmark suite show a reduction in power test applying (41% for s298) as well as a reduction in power test vector inserting (25% for s298).

VI. Proposed Method

Clustering of Paths to Reduce the Test set Size

In the adaptive testing approach, a set of test patterns is prepared for each process condition. During testing, a testing machine applies a set of test patterns (i.e., a test program) according to the identified process condition of a given circuit. Although adaptively can reduce redundant test patterns, it requires large memory space on a testing machine to store test patterns for each process condition. In practice, the memory space on a testing machine is limited; hence process conditions with their corresponding test patterns must be clustered. Clustering of process conditions saves memory on the testing machine but typically results in redundant test patterns for any given process condition in a cluster.

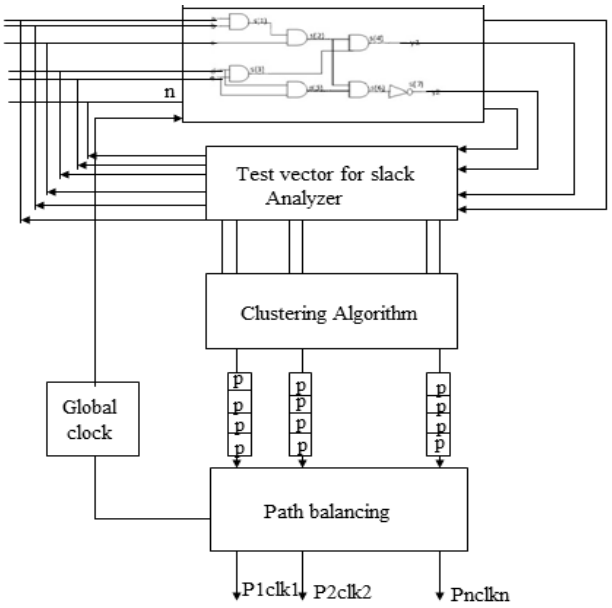

Fig. 5. Clustering of paths to eliminate delay errors.

The nominal delay of the paths is calculated and will be clustered based on similar path delays as shown in Fig (5). The longest delay path is predicted and all the remaining path delays are dynamically tuned to match the longest path delay with the help of ADPLL. The CUT will be recharacterized to prove that the path adjustment algorithm reduces delay errors. By this method the power consumption is reduced and reliability is enhanced.

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VII. Simulation Result

1) Variable PLL model

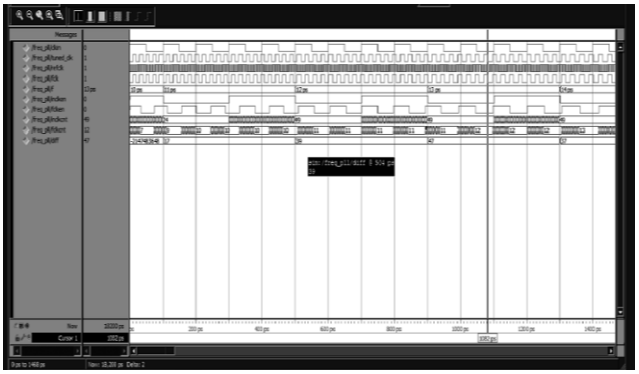

Fig. 6. Tuned path output of frequency detector.

The output of frequency detector how the delay is reduced using ADPLL using AC - Plus Scan**.**

2) Path Delay Calculation Using Benchmark Circuit

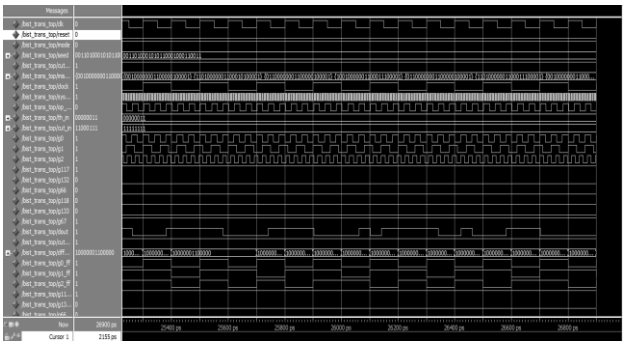

Fig. 7. Delay calculation using Benchmark circuit.

The small delay path from source to destination is calculated and obtained using Benchmark circuit.

3) RTL Diagram for s298 Circuit

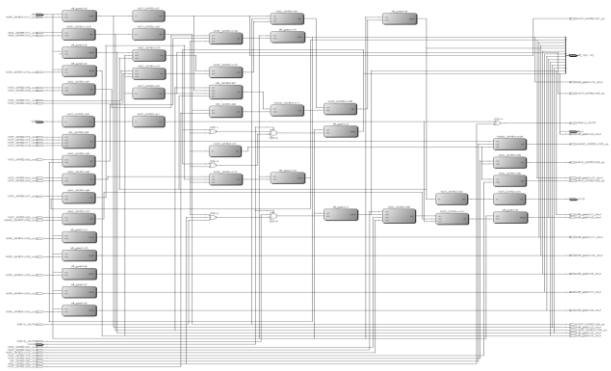

Fig. 8. RTL diagram of Benchmark circuit.

VIII. Conclusion

An adaptive PLL circuit with clock controlled logic is designed and employed for AC-plus scan testing. The chip parameters are based on the no of errors patterns. The target, middle and contour clock periods are computed using delay and unreliability score. The small delay defect in the circuit under test will be detected and characterized using three types of testing methodology. An s298 benchmark circuit is selected as testing CUT due to its adaptability in both combinational and sequential testing procedures. The input pattern to the benchmark circuit is generated under three different frequency ranges and the characterization is done based on its error rate under all the clock periods. As by our experiment the s298 circuit is classified as marginal chip since it passes the target clock period and produces delay errors in middle and contour clock periods.

Table I

Existing Timing Summary

Timing Analyzer Summary			
Type	Slack	Required Time	Actual Time
Worst-case tsu	N/A	None	5.175 ns
Worst-case tco	N/A	None	6.637 ns
Worst-case th	N/A	None	3.549 ns
Clock Setup: 'clk'	N/A	None	Restricted to 420.17 MHz (period = 2.380 ns)
Total number of failed paths			

Table II

Proposed Timing Summary

Timing Analyzer Summary			
Type	Slack	Required Time	Actual Time
Worst-case tsu	N/A	None	4.154 ns
Worst-case tco	N/A	None	8.059 ns
Worst-case th	N/A	None	0.492 ns
Clock Setup: 'clk'	N/A	None	Restricted to 420.17 MHz (period = 2.380 ns)
Total number of failed paths			

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IX. Future Work

The AC plus scan methodology can be modified not only to detect delay defects but also to correct the defects with adaptive frequency path using clustering algorithm. Based on the characterization of the chip condition, if the probability of the delay occurrences is low then it can be reconfigured to adjust its operating frequency to eradicate the delay defects. Individual path frequencies can be changed using path clustering to remove the delay difference in the depended paths which will affect the overall power and error performances.

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Authors Bibliography

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